IN THE CLAIMS

Please amend the claims as follows:

1. (original) Integrated circuit having a plurality of processing modules (I, T), wherein at least one first processing module (I) issues at least one transaction towards at least one second processing module (T), comprising:

at least one first transaction retraction unit (TRU1) for indicating the allowance to said at least one first of said processing modules (I) to retract said at least one transaction according to the state of said second processing module (T).

2. (original) Integrated circuit according to claim 1, wherein

said at least one first transaction retraction unit (TRU1) is associated to said at least one second processing module (T),

3. (currently amended) Integrated circuit according to claim 1~~or 2~~, further comprising

at least one second transaction retraction unit (TRU2) being associated to said first processing module for issuing an explicit transaction retraction request (rt) to said first transaction retraction unit (TRU1) or said second processing module (T),

wherein said first transaction retraction unit (TRU1)

indicates the allowance of said transaction retraction request (rt).

4. (original) Integrated circuit according to claim 3, wherein said first transaction retraction unit (TRU1) indicates the allowance of said transaction retraction request (rt), if the transaction retraction request (rt) is present.

5. (currently amended) Integrated circuit according to claim 1~~or 2~~, further comprising

at least one second transaction retraction unit (TRU2) being associated to said first processing module for issuing an explicit transaction retraction request (rt) to said first transaction retraction unit (TRU1) or said second processing module (T),

wherein said first transaction retraction unit (TRU1) indicates an allowance of said transaction retraction request (rt), if a valid command (CMD) issued from said first processing module (I) is present, the valid command (CMD) has not been accepted by the second processing module (T), and the transaction retraction request (rt) is present.

6. (currently amended) Integrated circuit according to claim 1~~or 2~~, wherein

said first retraction unit (TRU1) indicates an allowance of a requested transaction retraction, if a valid command (CMD) issued from said first processing module (I) is present, and the valid command (CMD) has not been accepted yet by the second processing module (T).

7. (original) Method for transaction retraction in an integrated circuit having a plurality of processing modules (I, T), comprising the steps of:

issuing at least one transaction by at least one first processing module (I) towards at least one second processing module (T),

indicating the allowance to retract said at least one transaction according to the state of said second processing module (T) to said at least one first of said processing modules (I).

8. (original) Data processing system, comprising

a plurality of processing modules (I, T), wherein at least one first processing module (I) issues at least one transaction towards at least one second processing module (T), comprising:

at least one first transaction retraction unit (TRU1) for indicating an allowance to said at least one first of said

processing modules (I) to retract said at least one transaction according to the state of said second processing module (T).